UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,422	09/20/2000	Bin Zhao		7422

25700 7590 12/16/2003

FARJAMI & FARJAMI LLP
16148 SAND CANYON
IRVINE, CA 92618

EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/665,422	ZHAO ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,21 and 24-28* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated by Zhao (US Pat. No. 6,211,561 B1).

3. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Zhao teaches a method of forming a semiconductor device comprising the steps of:

a) fabricating the damascene structure (see the structure shown in figure 4) to a via level (16) (see fig. 5) through a processing step prior to forming contact vias (30) (see fig. 9), wherein step (a) comprises:

i. depositing a first dielectric layer (18) (see fig. 3A), and

ii. depositing a first capping layer (60) over the first dielectric layer (18) (see fig. 3B) (please note that the reference sign 18 in figure 3C represents the combination of the layers 18 and 60, see col. 5, lines 39-41);

b) etching one or more air trenches (22) into the damascene structure so that the air trenches are positioned between selected metal lines (16) (see fig. 5); and

c) depositing a sealing layer (26) over the damascene structure having air trenches (22) to seal the air trenches (see fig. 6).

Regarding claim 21, Zhao teaches a method of forming a semiconductor device comprising the steps of:

a) fabricating the damascene structure (see the structure shown in figure 31B) to a via level (16) (see fig. 31B) through a processing step prior to forming contact vias (30C) (see fig. 31B);

b) etching one or more air trenches (22C) into the damascene structure so that the air trenches are positioned between selected metal lines (16) (see fig. 31B); and

c) depositing a sealing layer (26C) over the damascene structure having air trenches (22C) to seal the air trenches (see fig. 31B); and

d) depositing a polish stop layer (19D) over the damascene structure having air trenches (22C) to seal the air trenches (see fig. 31B).

4. Claims 1 and 4-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (US Pat. No. 6,159,840).

Regarding claim 1, Wang teaches a method of forming a semiconductor device comprising the steps of:

a) fabricating the damascene structure (see the structure shown in figure 2A) to a via level (202) (see fig. 2A) through a processing step prior to forming contact vias (220a) (see fig. 2F), wherein step (a) comprises:

i. depositing a first dielectric layer (204) (see fig. 2A), and

ii. depositing a first capping layer (206) over the first dielectric layer (204) (see fig. 2A);

b) etching one or more air trenches (212b) into the damascene structure so that the air trenches are positioned between selected metal lines (202) (see fig. 2B); and

c) depositing a sealing layer (214) over the damascene structure having air trenches (212b) to seal the air trenches (213) (see fig. 2C).

Regarding claim 4, Wang further teaches the steps of: forming a via (212a) in the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over[1] the sealing layer (214) (see fig. 2E); forming a conductive layer (220) in the trench (218) (see fig. 2F); and forming a metal plug (220a) in the via (212a) (see fig. 2F).

[1] With regards to the limitations of "forming a trench over the sealing layer" and "forming a trench over the etch stop layer", as recited in claims 4-8 and 24-28, and now rejected under 35 U.S.C §102(e) and 35 U.S.C 103(a) in view of Wang (US 6,159,840), the examiner interpreted the preposition "over" to mean ***throughout***, according to the Merriam-Webster's Collegiate Dictionary, 10th ed., meaning ***6a*** of the second definition of the term over.

Regarding claim 5, Wang further teaches the steps of: depositing an etch stop layer (216) over the sealing layer (214) (see fig. 2D); forming a via (212a) in the etch stop layer, the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the etch stop layer (214) (see fig. 2E); forming a conductive layer (220) in the trench (218) (see fig. 2F); and forming a metal plug (220a) in the via (212a) (see fig. 2F).

Regarding claims 6-8, Wang further teaches the steps of: forming a via[2] (212a) in the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the sealing layer (214) (see fig. 2E); and forming a conductive layer (220) in the trench (218) (see fig. 2F).

5. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated by Ghoshal (US Pat. No. 6,204,165 B1).

Regarding claim 1, Ghoshal teaches a method of forming a semiconductor device comprising the steps of:

a) fabricating the damascene structure (see the structure shown in figure 4A) to a via level through a processing step prior to forming contact vias (consider the via 171 between layers 159 and 161 in fig. 4A), wherein step (a) comprises:

i. depositing a first dielectric layer (115) (see fig. 4A), and

ii. depositing a first capping layer (135) over the first dielectric layer (115) (see fig. 4A)

b) etching one or more air trenches (410) into the damascene structure so that the air trenches (410) are positioned between selected metal lines (155 and 159) (see fig. 4F); and

c) depositing a sealing layer (430) over the damascene structure having air trenches (410) to seal the air trenches (see fig. 4G).

Regarding claim 2, Ghoshal further teaches that the step (a) comprises the following steps:

iii. (a_3) depositing a second capping layer (136) over the first capping layer (135) (see fig. 4A),

iv. (a_4) depositing a second dielectric layer (117) over the second capping layer (136) (see fig. 4A); and

v. (a_5) depositing a third capping layer (137) over the second dielectric layer (117) (see fig. 4A).

Regarding claim 3, Ghoshal further teaches etching an air trench (410) in the first (115) and second (117) dielectric layers and the first (135), second (136) and third (137) capping layers (see fig. 4G).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

---

[2] With regards to claims 6 and 26, the examiner interpreted the limitations "forming a via in the sealing layer" and "forming a via in the damascene structure" as ***one*** step describing the same via or opening formed throughout the structure.

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 21 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US Pat. No. 6,159,840) in view of Grill et al. (US 2002/0127844 A1).

Regarding claim 1, Wang teaches a method of forming a semiconductor device (see figure 2G) comprising the steps of: (a) fabricating the damascene structure (see the structure shown in figure 2A) to a via level (202) (see fig. 2A) through a processing step prior to forming contact vias (220a) (see fig. 2F); (b) etching one or more air trenches (212b) into the damascene structure so that the air trenches are positioned between selected metal lines (202) (see fig. 2B); and (c) depositing a sealing layer (214) over the damascene structure having air trenches (212b) to seal the air trenches (213) (see fig. 2C). In addition, Wang teaches the step of forming a conductive layer (220) over the sealing layer (214) (see fig. 2F).

However, Wang fails to teach the step (d) depositing a polish stop layer over the sealing layer. Grill et al. teaches that is well known in the art to provide a barrier or polish stop layer (170) before to depositing the conductive layer (185) (see figures 1D and 1E).

Wang and Grill et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a polish stop layer over the sealing layer prior to form the conductive layer. The motivation for doing so, as is taught by Grill et al., is to provide a protective material that is resistant to the reactive species used in the etch-back step (e.g. CMP) (paragraph [0041], last sentence and paragraph [0044], first sentence). Therefore, it would have been obvious to combine Grill et al. with Wang to obtain the invention of claims 21 and 24-28.

Regarding claim 24, Wang further teaches the steps of: forming a via (212a) in the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the sealing layer (214) (see fig. 2E); forming a conductive layer (220) in the trench (218) (see fig. 2F); and forming a metal plug (220a) in the via (212a) (see fig. 2F).

Regarding claim 25, Wang further teaches the steps of: depositing an etch stop layer (216) over the sealing layer (214) (see fig. 2D); forming a via (212a) in the etch stop layer, the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the etch stop layer (214) (see fig. 2E); forming a conductive layer

(220) in the trench (218) (see fig. 2F); and forming a metal plug (220a) in the via (212a) (see fig. 2F).

Regarding claims 26-28, Wang further teaches the steps of: forming a via (212a) in the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the sealing layer (214) (see fig. 2E); and forming a conductive layer (220) in the trench (218) (see fig. 2F).

Allowable Subject Matter

9. Claims 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a method for fabricating a damascene interconnect structure comprising the steps of: etching one or more air trenches into a damascene structure so that the air trenches are positioned between selected metal lines, and wherein the damascene structure comprises a first dielectric layer, a first capping layer over the first dielectric layer, a second capping layer over the first capping layer, a second dielectric layer over the second capping layer, a third capping layer over the second dielectric layer; and depositing a polish stop layer over the sealing layer formed over the damascene structure.

Response to Arguments

11. Applicant's arguments with respect to claims 1-21 and 24-28 have been considered but are moot in view of the new ground(s) of rejection. With regards to arguments against the dielectric layer (214) of Wang, it seems that applicant has overlooked the description disclosed in applicant's specification, in which the sealing layer is defined as to be merely a dielectric layer deposited over an air gap (see page 10, lines 6-13 of applicant's specification). Wang clearly fulfills this definition by teaching a dielectric layer (214) deposited over an air gap (213) (see fig. 2C). Therefore, applicant's arguments are not persuasive since the layer (214) of Wang is in fact a "sealing" layer.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach a method of forming air gap: Lin et al. (US Pat. Nos. 6,211,057 B1 and 6,130,151), Sasaki (US Pat. No. 6,064,118), Sun (Us Pat. No. 6,350,672 B1), and Nag et al. (US Pat. No. 6,297,125 B1).

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078 or (571) 272-1727, after February 9, 2004. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TOM THOMAS
SUPERVISORY PATENT EXAMINER

JRD